Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Cancelled)

2. (New) A semiconductor device, comprising:

a first chip comprising a nonvolatile memory cell having a plurality of first memory cells and a first portion of a peripheral circuit dedicated to the plurality of first memory cells; and

a second chip electrically connected to the first chip and comprising a plurality of second memory cells and a second portion of a peripheral circuit dedicated to the plurality of first memory cells.

3. (New) The semiconductor device of claim 2, wherein the plurality of second memory cells comprise:

a random access memory.

4. (New) The semiconductor device of claim 3, wherein the second portion of the peripheral circuit comprises:

an error detection/correction circuit.

5. (New) The semiconductor device of claim 2, wherein the second portion of the peripheral circuit comprises:

an interface circuit.

6. (New) The semiconductor device of claim 2, wherein the second portion of the peripheral circuit comprises:

a portion of a control circuit configured to control said plurality of first memory cells.

7. (New) The semiconductor device of claim 3, wherein the first chip further comprises:

a voltage boost circuit for the plurality of first memory cells.

8. (New) The semiconductor device of claim 2, wherein the second portion of the peripheral circuit comprises:

a circuit configured to read a flag identifying an error in said plurality of first memory cells.

9. (New) The semiconductor device of claim 2, wherein one of said plurality of first memory cells comprises:

a two-layered gate structure, including a control gate and a floating gate; and

a MOS transistor has one-layered gate structure.

10. (New) The semiconductor device of claim 2, wherein the plurality of first memory cells comprise:

a NAND structure shared by source/drain regions of adjacent transistors.

11. (New) The semiconductor device of claim 2, wherein the random access memory comprises one of:

an SRAM,

a pseudo-SRAM, and

a DRAM.

12. (New) The semiconductor device of claim 2, wherein the nonvolatile memory cell comprises one of

a NAND-type flash memory,

an AND-type flash memory,

a DINOR-type flash memory, and

a NOR-type flash memory.

13. (New) The semiconductor device of claim 2, wherein the first chip is arranged in parallel with the second chip.

14. (New) The semiconductor device of claim 2, wherein the first chip and the second chip are stacked on each other.

15. (New) A memory, comprising:

a first chip comprising a nonvolatile memory cell having a plurality of first memory cells and a first portion of a peripheral circuit dedicated to the plurality of first memory cells; and

a second chip electrically connected to the first chip and comprising a plurality of second memory cells and a second portion of a peripheral circuit dedicated to the plurality of first memory cells, wherein

said first and second chips are arranged on one of a memory card and a multi-chip-package.

16. (New) The memory of claim 15, wherein the second memory cells comprise:

a random access memory.

17. (New) The memory of claim 15, wherein the second portion of the peripheral circuit comprises:

an error detection/correction circuit.

18. (New) The memory of claim 15, wherein the second portion of the peripheral circuit comprises:

an interface circuit.

19. (New) The memory of claim 15, wherein the second portion of the peripheral circuit comprises:

a portion of a control circuit configured to control said plurality of first memory cells.

20. (New) The memory of claim 16, wherein the first chip comprises:

a voltage boost circuit for the plurality of first memory cells.

21. (New) The memory of claim 15, wherein the second portion of the peripheral circuit comprises:

a circuit configured to read a flag identifying an error of the plurality of first memory cells.

22. (New) The memory of claim 15, wherein the nonvolatile memory cell comprises:

a two-layered gate structure, including a control gate and a floating gate; and

a MOS transistor has one-layered gate structure.

23. (New) The memory of claim 15, wherein the first memory cells comprise:

a NAND structure shared by source/drain regions of adjacent transistors.

24. (New) The memory of claim 15, wherein the random access memory comprises one of:

an SRAM,

a pseudo-SRAM, and

a DRAM.

25. (New) The memory of claim 15, wherein the nonvolatile memory cell comprises one of:

a NAND-type flash memory,

an AND-type flash memory,

a DINOR-type flash memory, and

a NOR-type flash memory.

26. (New) The memory of claim 15, wherein the first chip is arranged in parallel with the second chip.

27. (New) The memory of claim 15, wherein the first chip and the second chip are stacked on each other.